

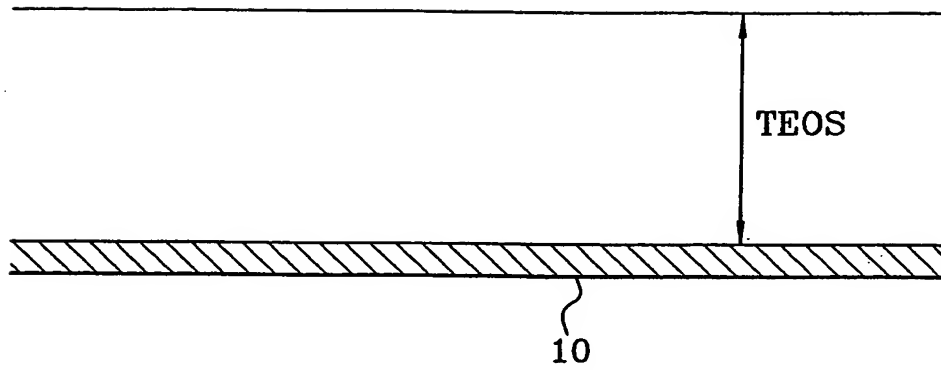
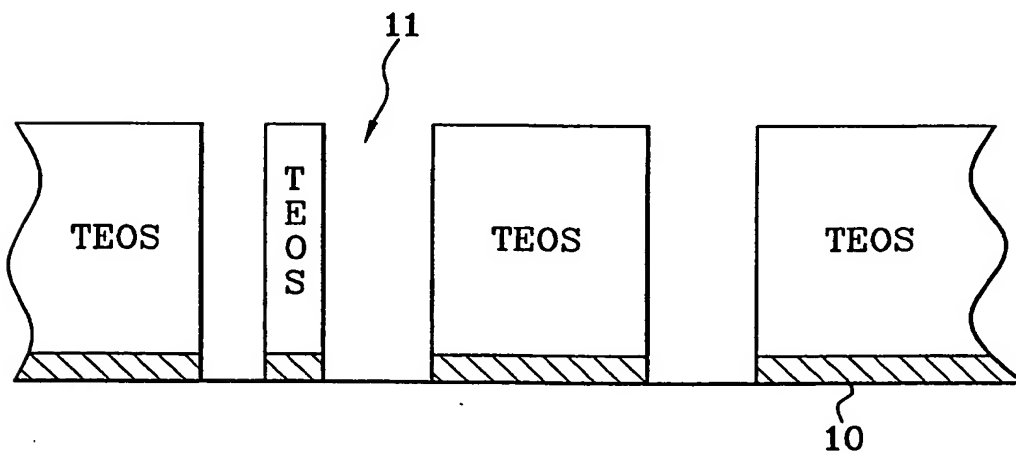
Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate with a central gate structure (1) and two side gate structures (5). A TEOS layer (6) is deposited over the gates. Electrodes (elec1, elec2) are formed on the TEOS layer. A top layer (2) is on the left, and a bottom layer (4) is on the right. A central channel (3) is defined by the gates.

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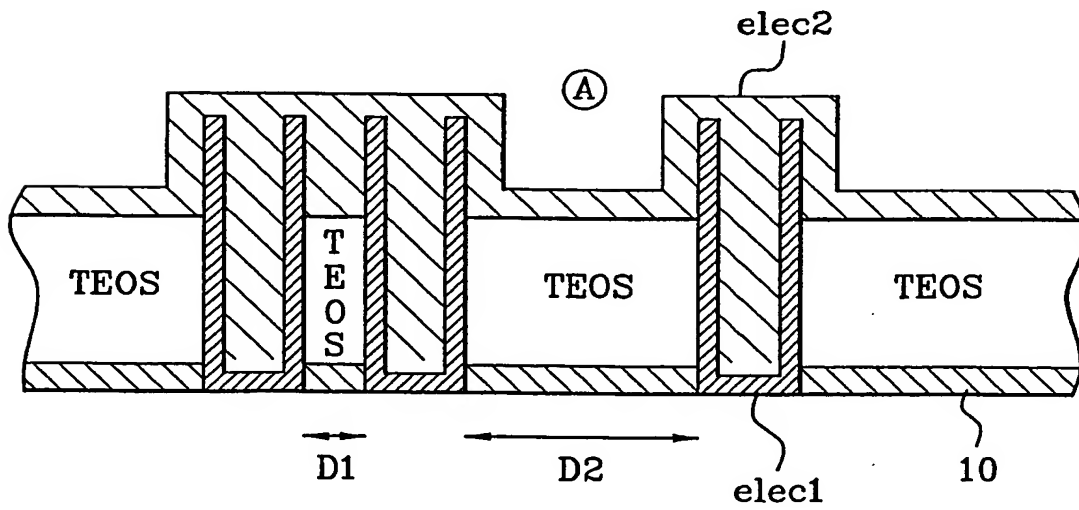
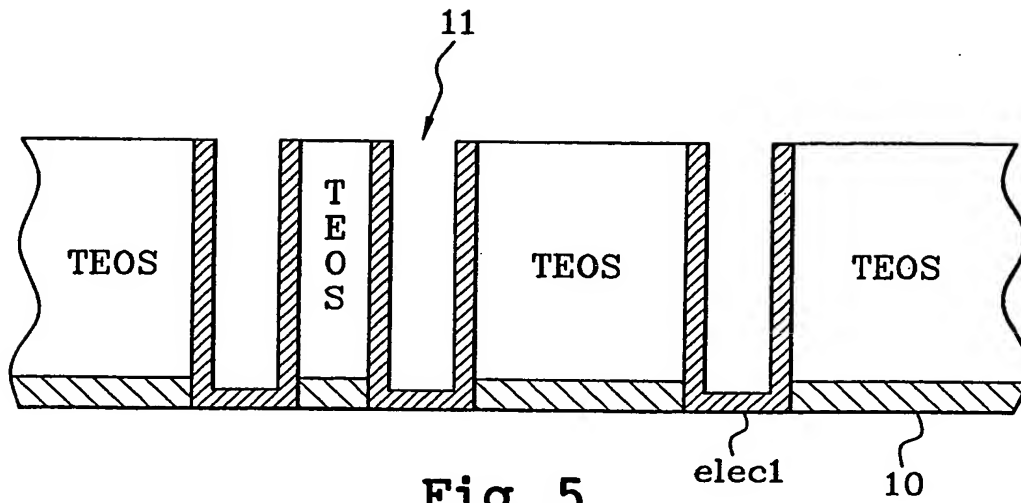


Fig. 2  
(PRIOR ART)

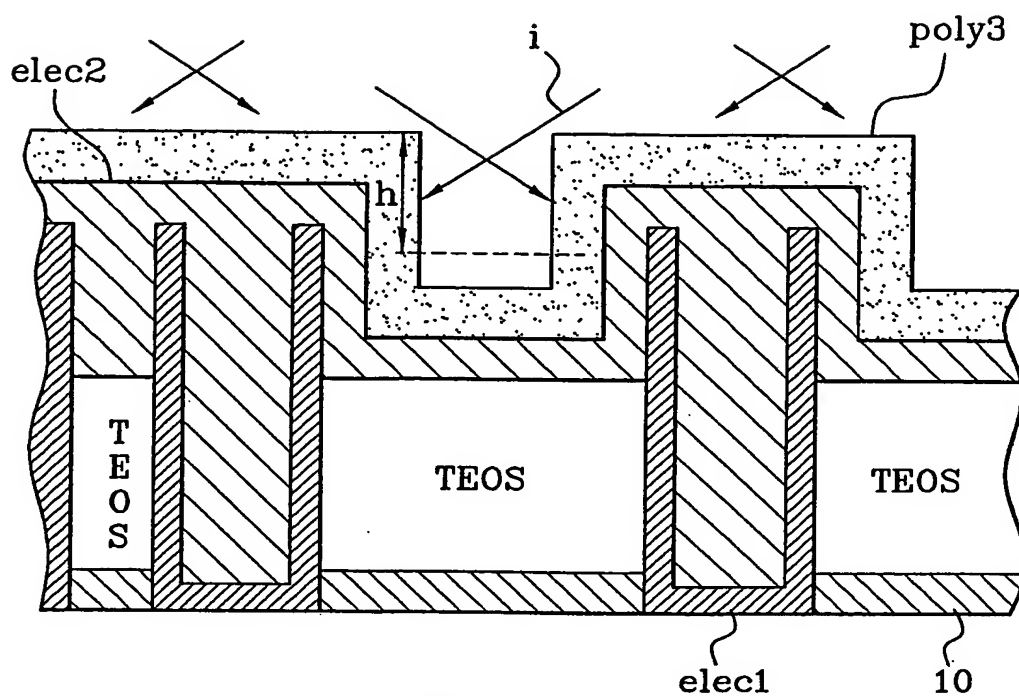
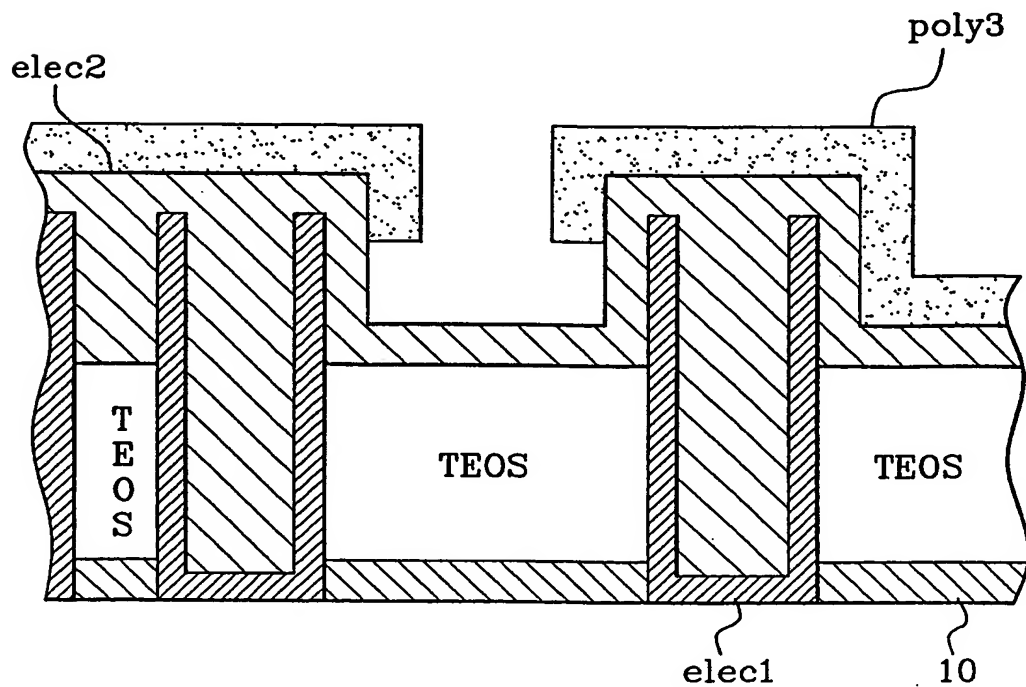
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Fig. 3Fig. 4

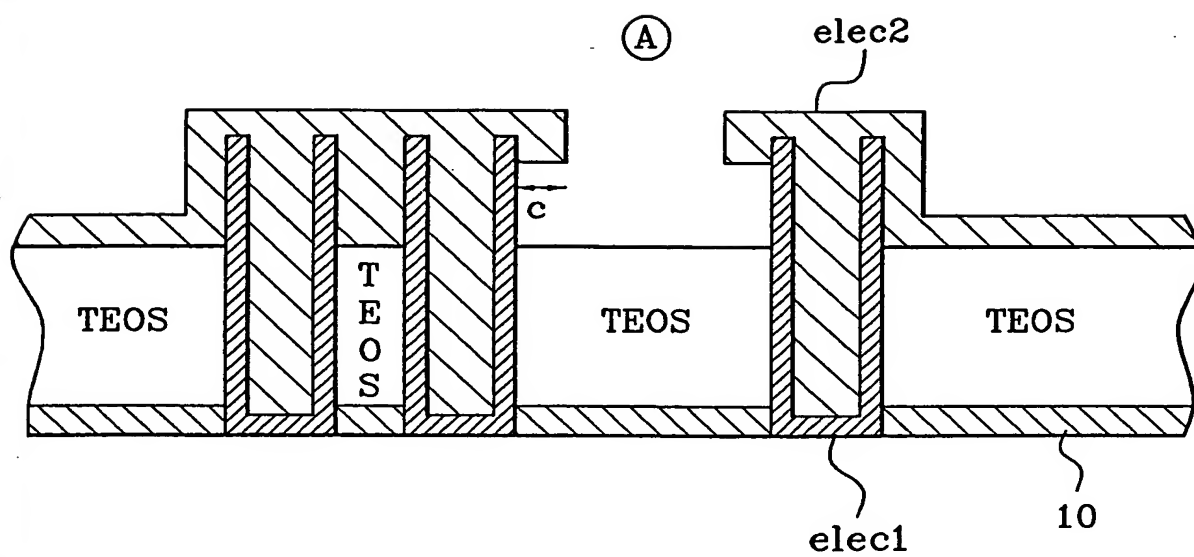
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Fig. 7Fig. 8

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Fig. 9